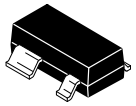
ASM161, ASM162

μP Supervisory Circuit

ON Semiconductor®

http://onsemi.com



SOT−143
4 LEAD
CASE 527AF

Description

The ASM161 and ASM162 are cost effective, low power supervisory circuits that monitor power supplies in microprocessor, microcontroller and digital systems. If the power supply drops below the reset threshold level, a reset is asserted and remains asserted for at least 800 ms after V_{CC} has risen above the reset threshold. An improved manual reset architecture gives the system designer additional flexibility.

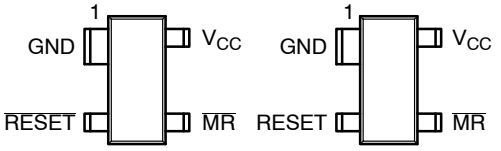
The debounced manual reset input is negative edge triggered. The reset pulse period generated by a MR transition is a minimum of 800 ms and a maximum of 2 sec duration. In addition, The $\overline{MR}$ input signal is blocked for an additional 49 μS minimum after the reset pulse ends. During the $\overline{MR}$ disable period, the microcontroller is guaranteed a time period free of additional manual reset signals. During this period DRAM contents can be refreshed or other critical system tasks undertaken. Low power consumption makes the ASM161/162 ideal for use in portable and battery operated equipments. With 3 V supplies, power consumption is 8 μW typically and 30 μW maximum. The ASM161 has an open−drain, active−LOW $\overline{RESET}$ output and requires an external pull−up resistor. The ASM162 has an active HIGH RESET output.

The ASM161/162 are offered in compact 4−pin SOT−143 packages. No external components are required to trim threshold voltage for monitoring different supply voltages. With six different factory set, reset, threshold ranges from 2.63 V to 4.63 V, the ASM161/162 are suitable for monitoring 5 V, 3.6 V and 3.0 V supplies. The ASM161/162 are available in temperature ranges 0°C to 70°C and −40°C to +85°C.

Features

- Edge Triggered Manual Reset Input
- Single Pulse Output
- 49 μS Minimum $\overline{MR}$ Disable Period After Reset
- CMOS/TTL Logic or Switch Interface
- Debounced Input
- Low Supply Current Extends Battery Life
  6 μA / 15 μA typ/max at 5.5 V
  4.5 μA / 10 μA typ/max at 3.6 V
- Long Reset Period
- 0.8 Sec Minimum, 2 Sec Maximum
- Two Reset Polarity Options
  ASM161: Active LOW, Open−drain
  ASM162: Active HIGH
- Pinout Matches the ASM811/812
- Small 4−Pin SOT−143 Package
- Two Temperature Ranges: 0°C to 70°C and −40°C to +85°C

PIN CONFIGURATIONS



$\overline{RESET}$ is open drain

RESET THRESHOLD

Part Suffix	Voltage (V)
L	4.63
M	4.38
J	4.00
T	3.08
S	2.93
R	2.63

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Applications

- PDAs
- Appliances
- Computers and Embedded Controllers
- Wireless Communication Systems
- Battery Operated and Intelligent Instruments
- Automotive Systems
- Safety Systems

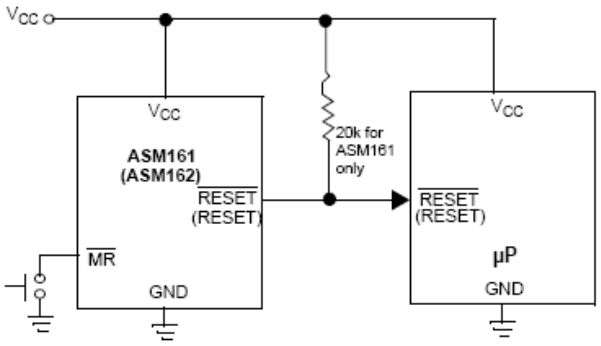


Figure 1. Typical Operating Circuit

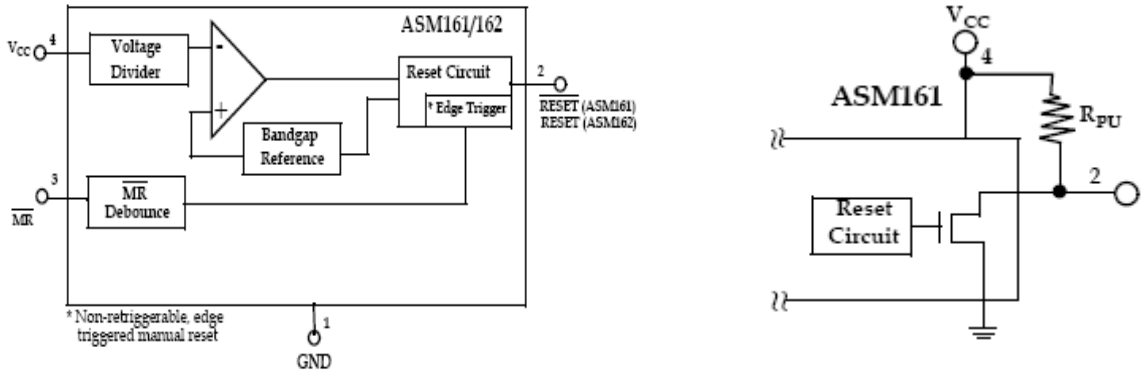


Figure 2. Block Diagram

Table 1. PIN DESCRIPTION

Pin #		Pin Name	Function
ASM161	ASM162		
1	1	GND	Ground.
2	–	$\overline{\text{RESET}}$	Active−LOW, open−drain reset output. $\overline{\text{RESET}}$ remains LOW while V_{CC} is below the reset threshold and for 800 ms minimum after V_{CC} rises above the reset threshold. An external pull−up resistor is needed.
–	2	RESET	Active HIGH reset output. RESET remains HIGH while V_{CC} is below the reset threshold and for 800 ms after V_{CC} rises above the reset threshold.
3	3	$\overline{\text{MR}}$	Manual reset input. A negative going edge transition on $\overline{\text{MR}}$ asserts reset. Reset remains asserted for one reset time−out period (800 ms min). This active−LOW input has an internal pull−up resistor. It can be driven from a TTL or CMOS logic line or shorted to ground with a switch. Leave open if unused.
4	4	V_{CC}	Power supply input voltage.

Detailed Description

The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure.

Reset Timing

A reset is generated whenever the supply voltage is below the threshold level ($V_{CC} < V_{TH}$). The reset duration is at least 800 ms after V_{CC} has risen above the reset threshold and is guaranteed to be no more than 2 seconds. The rest signal remains active as long as the monitored supply voltage is below the internal threshold voltage.

The ASM161 has an open−drain, active LOW $\overline{\text{RESET}}$ output (which is guaranteed to be in the correct state for V_{CC} down to 1.1 V). The ASM161 uses an external pull−up resistor. Output leakage current is under 1 µA. A high resistance value can be used to minimize current drain.

The ASM162 generates an active−HIGH RESET output.

Part Number	Reset Polarity
ASM161	LOW (use external pull−up resistor)
ASM162	HIGH

Manual Reset

The ASM161/162 have a unique manual reset circuit. A negative going edge transition on $\overline{MR}$ initiates the reset. A manual reset generates a single reset pulse of fixed length. The output−reset pulse remains asserted for the Reset Active Time−Out Period t_{RP} and then clears. Once the reset pulse is completed, the $\overline{MR}$ input remains disabled for at least 49 μS but not more than 122 μS. This period is specified as t_{MRD}.

During the $\overline{MR}$ disabled period, the microcontroller is guaranteed a time period free of new manual reset signals. This period can be used to refresh critical DRAM contents or other system tasks.

The $\overline{MR}$ pin must be taken HIGH and LOW again after the t_{MRD} period has been completed to initiate another reset pulse.

The manual reset input has an internal 20 kΩ pull−up resistor. $\overline{MR}$ can be left open if not used.

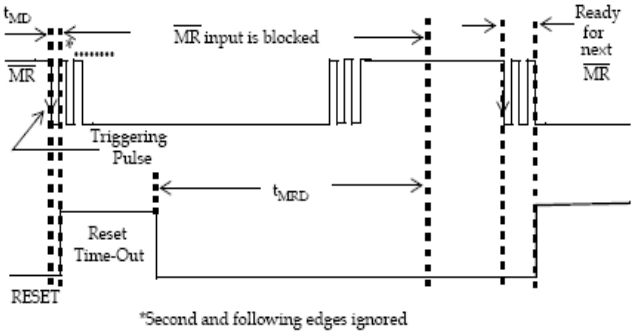


Figure 3. Manual Reset Timing

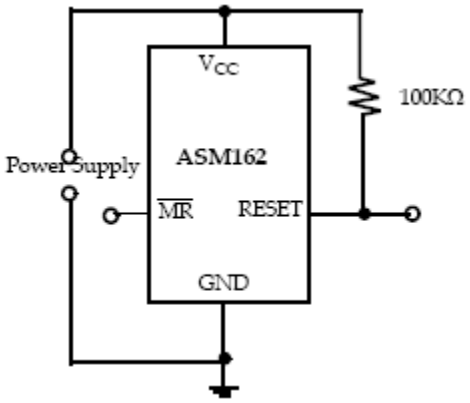


Figure 4. RESET Valid with VCC under 1.1 V

Application Information

Glitch Resistance

The ASM161/162 are relatively immune to short duration negative−going VCC transients/glitches. A VCC transient that goes 100 mV below the reset threshold and lasts 20s or less will not typically cause a reset pulse.

Valid Reset with VCC under 1.1 V

To ensure that logic inputs connected to the ASM162 RESET pin are in a known state when VCC is under 1.1 V, a 100 kΩ pull−down resistor at RESET is needed. The value is not critical.

This scheme does not work with the open−drain outputs of ASM161.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Pin Terminal Voltage with Respect to Ground V_{CC} RESET, $\overline{RESET}$ and $\overline{MR}$ Input Current at VCC and $\overline{MR}$	 −0.3 −0.3	 6.0 V_{CC} + 0.3 20	 V V mA
Rate of Rise at VCC		100	V/μs
Power Dissipation (TA = 70°C)		320	mW
Operating Temperature Range	−40	85	°C
Storage Temperature Range	−65	160	°C
Lead Temperature (soldering, 10 sec)		300	°C
ESD rating HBM MM		 2 200	 KV V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

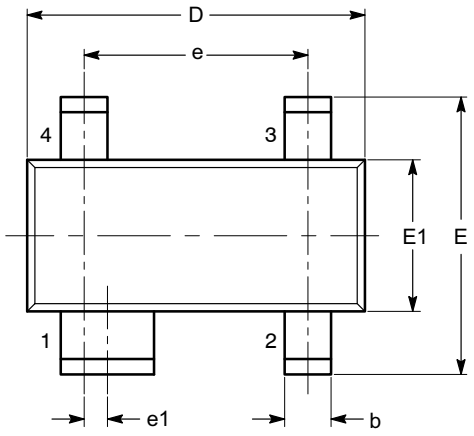
Table 3. ELECTRICAL CHARACTERISTICS
(Unless otherwise noted, V_{CC} is over the full range and T_A = 0°C to 70°C for ASM161/162 X C and T_A = −40°C to +85°C for ASM161/162 X E devices. Typical values at T_A = 25°C, V_{CC} = 5 V for L/M/J devices, V_{CC} = 3.3 V for T/S devices and V_{CC} = 3 V for R devices.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input Voltage (V_{CC}) Range	V_{CC}	T_A = 0°C to 70°C		1.1		5.5	V
Supply Current (Unloaded)	I_{CC}	T_A = 0°C to 70°C, T_A = −40°C to +85°C	V_{CC} < 5.5 V L/M/J		6	15	μA
		T_A = 0°C to 70°C, T_A = −40°C to +85°C	V_{CC} < 3.6 V R/S/T		4.5	10	
Reset Threshold	V_{TH}	L Devices	T_A = 25°C (Note 1)	4.56 4.50	4.63	4.70 4.75	V
		M devices	T_A = 25°C (Note 1)	4.31 4.25	4.38	4.45 4.50	
		J devices	T_A = 25°C (Note 1)	3.93 3.89	4.00	4.06 4.10	
		T devices	T_A = 25°C (Note 1)	3.04 3.00	3.08	3.11 3.15	
		S devices	T_A = 25°C (Note 1)	2.89 2.85	2.93	2.96 3.00	
		R devices	T_A = 25°C (Note 1)	2.59 2.55	2.63	2.66 2.70	
Reset Threshold Temp Coefficient	T_{CVTH}				30		ppm/°C
V_{CC} to reset delay		V_{CC} = V_{TH} to (V_{TH} −100 mV)			20		μS
Reset Pulse Width	t_{RPW}	T_A = 0°C to 70°C		800	1400	2000	ms
		T_A = −40°C to 85°C		600		2240	
$\overline{MR}$ Minimum Pulse Width	t_{MR}			10			μS
$\overline{MR}$ Glitch Immunity					100		ns
$\overline{MR}$ to RESET Propagation Delay					0.5		μS
$\overline{MR}$ Input Threshold	V_{IH}	V_{CC} > V_{TH}(MAX), L/M/J devices		2.3			V
	V_{IL}					0.8	V
	V_{IH}	V_{CC} > V_{TH}(MAX), R/S/T devices		0.7V_{CC}			V
	V_{IL}					0.25V_{CC}	V
$\overline{MR}$ Delay to $\overline{MR}$ Retrigger	t_{MRD}	T_A = 0°C to 70°C		48	85	122	μS
		T_A = −40°C to 85°C			85		
$\overline{MR}$ pull−up resistance				10	20	30	KΩ
Low $\overline{RESET}$ output voltage (ASM161)	V_{OL}	V_{CC} = V_{TH} min., I_{SINK} = 1.2 mA, ASM161 R/S/T				0.3	V
		V_{CC} = V_{TH} min., I_{SINK} = 3.2 mA, ASM161L/M/J				0.4	
		V_{CC} > 1.1, I_{SINK} = 50 μA				0.3	
RESET Output Voltage (ASM162)	V_{OL}	V_{CC} = V_{TH} max., I_{SINK} = 1.2 mA, ASM162 R/S/T				0.3	V
		V_{CC} = V_{TH} max., I_{SINK} = 3.2 mA, ASM162 L/M/J				0.4	
HIGH RESET Output Voltage (ASM162)	V_{OH}	1.8 < V_{CC} < $V_{THmin.}$, I_{SOURCE} = 150 μA		0.8V_{CC}			V

1. Over operating temperature range.

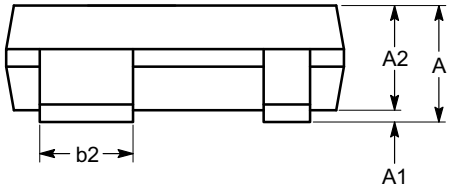
PACKAGE DIMENSIONS

SOT−143, 4 Lead
CASE 527AF−01
ISSUE A

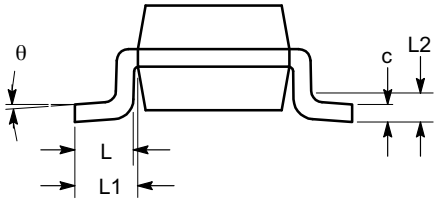


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.22
A1	0.05		0.15
A2	0.75	0.90	1.07
b	0.30		0.50
b2	0.76		0.89
c	0.08		0.20
D	2.80	2.90	3.04
E	2.10		2.64
E1	1.20	1.30	1.40
e	1.92 BSC		
e1	0.20 BSC		
L	0.40	0.50	0.60
L1	0.54 REF		
L2		0.25	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC TO-253.

Table 4. ORDERING INFORMATION

Part Number (Note 2)	**Reset Threshold (V)**	**Temperature (°C)**	**Pins−Package**	**Package Marking (LL Lot Code)**
TIN LEAD DEVICES				
ASM161LCUS/T	4.63	0 TO 70	4−SOT−143	TALL
ASM161MCUS/T	4.38	0 TO 70	4−SOT−143	TBLL
ASM161JCUS/T	4.00	0 TO 70	4−SOT−143	TCLL
ASM161TCUS/T	3.08	0 TO 70	4−SOT−143	TDLL
ASM161SCUS/T	2.93	0 TO 70	4−SOT−143	TELL
ASM161RCUS/T	2.63	0 TO 70	4−SOT−143	TFLL
ASM162LCUS/T	4.63	0 TO 70	4−SOT−143	TGLL
ASM162MCUS/T	4.38	0 TO 70	4−SOT−143	THLL
ASM162JCUS/T	4.00	0 TO 70	4−SOT−143	TILL
ASM162TCUS/T	3.08	0 TO 70	4−SOT−143	TJLL
ASM162SCUS/T	2.93	0 TO 70	4−SOT−143	TKLL
ASM162RCUS/T	2.63	0 TO 70	4−SOT−143	TLLL
ASM161LEUS/T	4.63	−40 TO 85	4−SOT−143	TMLL
ASM161MEUS/T	4.38	−40 TO 85	4−SOT−143	TNLL
ASM161JEUS/T	4.00	−40 TO 85	4−SOT−143	TOLL
ASM161TEUS/T	3.08	−40 TO 85	4−SOT−143	TPLL
ASM161SEUS/T	2.93	−40 TO 85	4−SOT−143	TQLL
ASM161REUS/T	2.63	−40 TO 85	4−SOT−143	TRLL
ASM162LEUS/T	4.63	−40 TO 85	4−SOT−143	TSLL
ASM162MEUS/T	4.38	−40 TO 85	4−SOT−143	TTLL
ASM162JEUS/T	4.00	−40 TO 85	4−SOT−143	TULL
ASM162TEUS/T	3.08	−40 TO 85	4−SOT−143	TVLL
ASM162SEUS/T	2.93	−40 TO 85	4−SOT−143	TWLL
ASM162REUS/T	2.63	−40 TO 85	4−SOT−143	TXLL
LEAD FREE DEVICES				
ASM161LCUSF/T	4.63	0 TO 70	4−SOT−143	MALL
ASM161MCUSF/T	4.38	0 TO 70	4−SOT−143	MBLL
ASM161JCUSF/T	4.00	0 TO 70	4−SOT−143	MCLL
ASM161TCUSF/T	3.08	0 TO 70	4−SOT−143	MDLL
ASM161SCUSF/T	2.93	0 TO 70	4−SOT−143	MELL
ASM161RCUSF/T	2.63	0 TO 70	4−SOT−143	MFLL
ASM162LCUSF/T	4.63	0 TO 70	4−SOT−143	MGLL
ASM162MCUSF/T	4.38	0 TO 70	4−SOT−143	MHLL
ASM162JCUSF/T	4.00	0 TO 70	4−SOT−143	MILL
ASM162TCUSF/T	3.08	0 TO 70	4−SOT−143	MJLL
ASM162SCUSF/T	2.93	0 TO 70	4−SOT−143	MKLL
ASM162RCUSF/T	2.63	0 TO 70	4−SOT−143	MLLL
ASM161LEUSF/T	4.63	−40 TO 85	4−SOT−143	MMLL
ASM161MEUSF/T	4.38	−40 TO 85	4−SOT−143	MNLL

2. For parts to be packed in Tape and Reel, add "−T" at the end of the part number. ON Semiconductor lead free parts are RoHS compliant.

Table 4. ORDERING INFORMATION (continued)

Part Number (Note 2)	Reset Threshold (V)	Temperature (°C)	Pins−Package	Package Marking (LL Lot Code)
LEAD FREE DEVICES				
ASM161JEUSF/T	4.00	−40 TO 85	4−SOT−143	MOLL
ASM161TEUSF/T	3.08	−40 TO 85	4−SOT−143	MPLL
ASM161SEUSF/T	2.93	−40 TO 85	4−SOT−143	MQLL
ASM161REUSF/T	2.63	−40 TO 85	4−SOT−143	MRLL
ASM162LEUSF/T	4.63	−40 TO 85	4−SOT−143	MSLL
ASM162MEUSF/T	4.38	−40 TO 85	4−SOT−143	MTLL
ASM162JEUSF/T	4.00	−40 TO 85	4−SOT−143	MULL
ASM162TEUSF/T	3.08	−40 TO 85	4−SOT−143	MVLL
ASM162SEUSF/T	2.93	−40 TO 85	4−SOT−143	MWLL
ASM162REUSF/T	2.63	−40 TO 85	4−SOT−143	MXLL

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PUBLICATION ORDERING INFORMATION

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ASM161/D